1. (Currently Amended) A method of forming a semiconductor latch for integrated circuits, said latch adapted to receive a first supply voltage and a second supply voltage substantially at a lower voltage level than said first supply voltage, the method comprised of:

fabricating a first inverter with logic transistors utilizing a first semiconductor layer, said first inverter fabrication comprising:

fabricating a first and a second conducting path of (a) the first inverter in (a) said first semiconductor layer, said first conducting path coupled between said first supply voltage and an output, said second conducting path coupled between said second supply voltage and said output; ~~and~~

depositing the logic transistor gate-dielectric layer on said first semiconductor layer;

depositing the logic transistor gate-poly silicon layer on said logic gate dielectric layer; and

fabricating gate regions in said gate-poly layer above a portion of said first and second conducting paths; and

depositing an isolation layer above said first inverter; and

fabricating a second inverter with thin film transistors (TFT) above the logic transistors utilizing a second semiconductor layer, said second inverter fabrication comprising:

depositing the second semiconductor layer on said isolation layer, substantially above said first semiconductor layer;

fabricating a first and a second conducting path of (a) the second inverter in (a) said second semiconductor layer, said first conducting path coupled between said first

supply voltage and an output, said second conducting path coupled between said second supply voltage and said output;

depositing the TFT gate-dielectric layer on said second semiconductor layer;

depositing the TFT gate-poly silicon layer on said TFT gate-dielectric layer; and

fabricating gate regions above a portion of said first and second conducting paths.

2. (As Filed) The method of claim 1, wherein said first semiconductor layer is one of substrate Silicon, amorphous Silicon, poly-crystalline Silicon, laser annealed poly-crystalline Silicon, compound semiconductor material, Silicon on insulator, and any other semiconductor material.

3. (As Filed) The method of claim 1, wherein said isolation layer is one of oxide, nitride, oxy-nitride, any dielectric material and any combination of dielectric materials.

4. (As Filed) The method of claim 1, wherein said second semiconductor layer is one of amorphous Silicon, poly-crystalline Silicon, laser annealed poly-crystalline Silicon, re-crystallized Silicon, compound semiconductor material and any other semiconductor material.

5. (As Filed) The method of claim 1, wherein said first and second conducting paths of said second inverter is fabricated on a single geometry of said second semiconductor layer.

6. (As Filed) The method of claim 1, further comprising:

forming a common gate for said first inverter, said gate modulating said first and second conducting paths of said first inverter to couple either said first supply voltage or said second supply voltage to said first inverter output; and

forming a common gate for said second inverter, said gate modulating said first and second conducting paths of said second inverter to couple either said first supply voltage or said second supply voltage to said second inverter output; and

coupling said output of first inverter to said common gate of second inverter; and

coupling said output of second inverter to said common gate of first inverter.

7. (Currently Amended) The method of claim 6, wherein said first inverter further comprises:

forming a pull-up transistor source region, channel region and a drain region in said first conducting path, said channel region formed between said source and drain regions, said source region coupled to said first supply voltage, said drain region coupled to said output; and

forming a pull-down transistor drain region, channel region and source region in said second conducting path, said channel region formed between said source and drain regions, said drain region coupled to said output, said source region coupled to said second supply voltage; and

~~depositing a dielectric layer on said first semiconductor layer and forming gate dielectric regions above channel regions for said pull-up and pull-down transistors; and~~

~~depositing a gate material on said dielectric layer, and~~ forming the gate regions above channel regions for said pull-up and pull-down transistors, and coupling both said gates together to form said common gate of first inverter.

8. (Currently Amended) The method of claim 6, wherein said second inverter is further comprised of:

forming a pull-up transistor source region, channel region and a drain region in said first conducting path, said channel region formed between said source and drain regions, said source region coupled to said first supply voltage, said drain region coupled to said output; and

forming a pull-down transistor drain region, channel region and source region in said second conducting path, said channel region formed between said source and drain regions, said drain region coupled to said output, said source region coupled to said second supply voltage; and

~~depositing a dielectric layer on said second semiconductor layer and forming gate dielectric regions above channel regions for said pull-up and pull-down transistors; and~~

~~depositing a gate material on said dielectric layer, and~~ forming the gate regions above channel regions for said pull-up and pull-down transistors, and coupling both said gates together to form said common gate of second inverter.

9. (Currently Amended) The method of claim 6, further comprising a pass-gate transistor comprised of:

forming a conducting path in said first semiconductor layer, said conducting path coupled between said common gate of ~~first~~ second inverter and a data line; and

forming a gate above said conducting path, said gate coupled to a row line, said gate at a first voltage level substantially coupling said data line to said common gate of ~~first~~ second inverter, said gate at a second voltage level substantially de-coupling said data line from said common gate of ~~first~~ second inverter.

10. (Currently Amended) The method of claim 6, further comprising a pass-gate transistor comprised of:

forming a conducting path in said second semiconductor layer, said conducting path coupled between said common gate of ~~second~~ first inverter and a data line; and

forming a gate above said conducting path, said gate coupled to a row line, said gate at a first voltage level substantially coupling said data line to said common gate of ~~second~~ first inverter, said gate at a second voltage level substantially de-coupling said data line from said common gate of ~~second~~ first inverter.

11. (As Filed) The method of claim 10, wherein said first and second conducting paths of said second inverter and said conducting path of said pass-gate transistor are fabricated on a single geometry of said second semiconductor layer.

12. (Currently Amended) A method of forming a semiconductor latch for integrated circuits, said latch adapted to receive a first supply voltage and a second supply voltage

substantially at a lower voltage level than said first supply voltage, the method comprising:

depositing an isolation layer above a first module layer, said first module comprising a high mobility semiconductor substrate layer used to fabricate logic transistors; and

depositing a semiconductor thin film layer; and

fabricating a first and a second conducting path of a first inverter in said semiconductor thin film layer, said first conducting path coupled between said first supply voltage and a first output, said second conducting path coupled between said second supply voltage and said first output; and

fabricating a first and a second conducting path of a second inverter in said semiconductor thin film layer, said first conducting path coupled between said first supply voltage and a second output, said second conducting path coupled between said second supply voltage and said second output.

13. (As Filed) The method of claim 12, wherein said isolation layer is one of oxide, nitride, oxy-nitride, any dielectric material and any combination of dielectric materials.

14. (As Filed) The method of claim 12, wherein said semiconductor thin film layer is one of amorphous Silicon, poly-crystalline Silicon, laser annealed poly-crystalline Silicon, re-crystallized Silicon, compound semiconductor material and any other semiconductor material.

15. (As Filed) The method of claim 12, wherein said first and second conducting paths of said first and second inverters are fabricated on a single geometry of said semiconductor thin film layer.

16. (As Filed) The method of claim 12, further comprising:

forming a common gate for said first inverter, said gate modulating said first and second conducting paths of said first inverter to couple either said first supply voltage or said second supply voltage to said first inverter output; and

forming a common gate for said second inverter, said gate modulating said first and second conducting paths of said second inverter to couple either said first supply voltage or said second supply voltage to said second inverter output; and

coupling said first output of first inverter to said common gate of second inverter; and

coupling said second output of second inverter to said common gate of first inverter.

17. (As Filed) The method of claim 16, wherein each of said first and second inverters further comprises:

forming a pull-up transistor source region, channel region and a drain region in said first conducting path, said channel region formed between said source and drain regions, said source region coupled to said first supply voltage, said drain region coupled to said inverter output; and

forming a pull-down transistor drain region, channel region and source region in said second conducting path, said channel region formed between said source and drain regions, said

drain region coupled to said inverter output, said source region coupled to said second supply voltage; and

depositing a dielectric layer on said semiconductor thin film layer and forming gate dielectric regions above channel regions for said pull-up and pull-down transistors; and

depositing a gate material on said dielectric layer, and forming gate regions above channel regions for said pull-up and pull-down transistors, and coupling both said gates together to form said common gate of said inverter.

18. (As Filed) The method of claim 16, further comprising a pass-gate transistor comprised of:

forming a conducting path in said semiconductor thin film layer, said conducting path coupled between a data line and one of said common gates of first or second inverter; and

forming a gate above said conducting path, said gate coupled to a row line, said gate at a first voltage level substantially coupling said data line to said common gate of inverter, said gate at a second voltage level substantially de-coupling said data line from said common gate of inverter.

19. (As Filed) The method of claim 18, wherein said first and second conducting paths of said first and second inverters and said conducting path of said pass-gate transistor are fabricated on a single geometry of said semiconductor thin film layer.

20. (Currently Amended) A method of fabricating a semiconductor latch for an integrated circuit, comprised of:

forming two inverters, said inverters cross-coupled to form a bi-stable latch; and

supplying each of said inverters with a first supply voltage and a second supply voltage, said second supply voltage substantially lower than said first supply voltage level, and

forming at least one of said inverters in a semiconductor thin film module, said module fabricated substantially above a semiconductor substrate module used to construct high performance switching logic circuits.

Please amend Fig-1A, Fig-1B, Fig-2A, Fig-2B, Fig-3A, Fig-3B, Fig-4, Fig-5, Fig-6A, Fig-6B, Fig-6C and Fig-7 as follows: